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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,385	02/05/2004	Donald E. Steiss	22347-08564 (8422)	6364

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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,385	STEISS ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-45 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-45 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-45, are rejected under 35 U.S.C. 103(a) as being unpatentable over Boggs (patent No. 7,051, 329) in view of Kalafatis (patent No. 6,785,890).

3. Boggs taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Fetch control unit (224,230) having an input coupled to receive an execution feedback signal (stall signal and mite stall) with information related to a plurality of threads on a per thread basis (e.g., see figs. 2,16,17,18), the fetch control unit generating an instruction fetch sequence based on the execution feedback signal (e.g., see col. 4, line 49-col. col. 5, line 66, and col. 6, line 52-66 and col. 11, lines 39-63); and

b) An instruction cache (212,214), having an input coupled on to an output of the fetch control unit (e.g., see fig. 2), the instruction cache dispatching instruction data responsive to the instruction fetch sequence (e.g., see col. 11, lines 39-63).

4. Boggs did not express detail (claims 1,16,31) the feedback signal with information related to a plurality of threads on a per thread basis. Kalafatis however taught (e.g., see fig.5), where the output from the thread allocation block of thread 0 and

thread 1 a single line is input to both inputs of the thread switching logic which would consistent with the single output from the thread allocation block provides for the information for plural threads. Also the thread switch signal (134) conveys the switch information for plural threads (e.g., see figs 5,6,15a).

5. It would have been obvious to one of ordinary skill in the art to combine the teachings of Boggs and Kalafatis. Both references were directed toward the problems of performing thread switching in a DP system (e.g., see col. 1, lines 16-34 of Boggs and col. 1, lines 16-20 of Kalafatis). One of ordinary skill would have been motivated to incorporate the several additional criteria and determination for switching threads such as on insufficient amount of decoded instructions to provide a system that could more effectively reduce processing time in a multithreaded processor (e.g., see abstract of Kalafatis).

6. As per claim 2,17,32 Boggs taught an instruction queue (238)(e.g., see col. 17, line 4-col. 18,line 1) having an output coupled to the fetch control unit input, the instruction queue generating a queue feed back signal responsive to a thread queue condition associated with a thread from the plurality of threads (e.g., see figs. 16, 17 and col. 1, line 1-col. 19, line 23).

7. Boggs however did not expressly detail (claim 2,17,32) wherein the fetch control unit generates the instruction fetch sequence also based on the queue feedback signal. Boggs taught switching thread in response queue feedback signals (e.g., see figs. 7,11,12,16,17). Since the processing of a thread would have required fetching of instructions for the active thread and would not bee needed for an inactive thread one of

ordinary skill would have been motivated to generate a fetch sequence based on the feedback (stall) signal (which indicated which thread is stalled and which thread is active) (e.g, see col. 20, line 45-col. 22, line 58). This also pertains to claims 5,20,35 where the Boggs thread switch would have provided for the fetch control unit blocking the thread from the fetch sequence responsive to queue feedback signal (that stalls the pipeline).

8. As per claims 3,18,33 Boggs taught wherein the thread queue condition indicates that a thread queue has less than a first amount of remaining storage (e.g., see col. 21, line 11-col. 22, lines 23).

9. As per claims 4,19,34 Kalafatis taught wherein the thread queue condition indicates that a thread queue has less than a second amount of remaining decoded instructions (e.g., see fig. 8 and 10 and 15B and col. 8, lines 1-56)[the amount of data chunks in instruction streaming buffer provide information for determine is a thread is switched where the streaming buffer would operate in first in first out manner].

10. As per claims 6,21,36 Boggs taught advancing the thread in the instruction fetch sequence responsive to the queue feedback signal (e.g., see figs. 13,14,15)[when the stall signal indication to not stall entries are allocated to the queue wherein the fetch portion of the system would have provided control to continue fetch required to continue processing a continuing thread would have a fetch control unit].

11. As per claims 7,22,37 Boggs taught a thread interleaver, the thread interleaver generating an interleaver feedback signal responsive to a thread condition, wherein the

fetch control unit generates the instruction fetch sequence also based on the interleaver feedback signal (fetch from one of multiple threads depending the feedback) (e.g., see fig. 9 and col. 9, line 7-col. 10, line 20 of Kalafatis)(also since the thread switch occurred due the feedback signal then the signal would have been coupled to fetch control unit to control the switching of threads so that the required fetching would have been performed only on the active thread).

12. As per claims 8,23,38 Boggs taught wherein the thread condition indicates that a thread from the plurality of thread is ineligible for execution (e.g., see fig. 9,15,16,17 of Boggs).

13. As per claims 9,24,39 Boggs taught wherein the thread interleaver generates a thread execution sequence independent of the instruction fetch sequence.(Kalafatis taught out of order execution of the instructions and replay of instructions and the queuing of instructions e.g., see fig. 2 and col. 5,lines 5-42 of Boggs) therefore the execution sequence would have been independent of the fetch sequence.

14. As per claims 10,25,40 Boggs taught an execution pipeline having an output coupled to the fetch control unit input (as discussed above), the execution pipeline generating the execution feedback signal responsive to an execution stall (e.g., see figs. 8, 9, ,10, 14,16).

15. As per claims 11,26,41 Boggs taught wherein the fetch control unit (as discussed above) delays the thread in the instruction fetch sequence responsive to an execution stall (e.g., see figs. 8, 9,10, 14,16).

16. As per claims 12,27,42 Kalafatis taught the execution stall comprises one from the group consisting of branch misprediction, an exception a data cache miss , an external resource stall, an interlock, and memory operation ordering (e.g., see figs. 6,9 and col. 13, lines 26-67).

17. As per claims 13,28,43 Kalafatis taught wherein the fetch control unit generates the instruction fetch sequence, in a default state, by selecting a thread from the plurality of threads according to round robin arbitration (with only two threads the switch from thread zero to thread one or vis versa would comprise round robin switching for two threads)(e.g., see fig. 8 of Kalafatis).

As per claims 14,29,44 Kalafatis taught wherein the execution feedback signal is capable of including information related to each of the plurality of threads (e.g., see fig.5, where the output from the thread allocation block of thread 0 and thread 1 a single line is input to both inputs of the thread switching logic which would be consistent with the single output from the thread allocation block provides for the information for plural threads.

18. As per claims 15,30,45 Kalafatis taught a multithreaded processor as discussed above. The application of a multi-threaded processor for processing multiple network thread would have provided a parallel processing of threads and therefore more efficient processing of the threads. Consequently one of ordinary skill in the DP art would have been motivated to apply the Boggs and Kalafatis system to processing network data and therefore provide a network processor which characteristically would process

packets in a routing switching bridging and forwarding operations which were conventional operations performed in networked processors.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Borkenhagen (patent No. 6,076,157) disclosed a system to force a thread switch in a multithreaded processor (e.g., see abstract).

Nageswaran (patent No. 6,991,792) disclosed a system for dynamically managing thread pool of reusable threads in a computer system (e.g., see abstract).

Bondi (patent No. 5,881, 277) disclosed pipelined microprocessor with branch misprediction cache circuits (e.g,. see abstract).

Merchant (patent No. 6,792,446) disclosed a system with storing of instructions relating to a stalled thread (e.g., see abstract).

Bunce (patent publication No. 2003/0163589 A1) disclosed a system for pipelined packet processing (e.g., see abstract).

Rodgers (patent No. 6,889,319) disclosed a system for entering and exiting multiple threads within a multithreaded processor (e.g., see abstract).

Kelsey (patent application publication (No. 2003/0037228) disclosed a system for instruction level multithreading scheduling in an embedded processor (e.g., see abstract).

Flynn (patent No. 5,907, 702) disclosed a system for decreasing thread switch latency in a multithreading processor (e.g., see abstract).

Bennett (Patent application publication No. 2003/0163675) disclosed context switching for a multi-thread execution pipeline loop method of operation (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

ERIC COLEMAN
PRIMARY EXAMINER